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10/733,302	12/12/2003	Junichi Tamura	OKI 402	7322

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EXAMINER	
THOMAS, SHANE M	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,302	TAMURA, JUNICHI	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/24/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed 9/24/2007. Claims 1-14 are pending. Applicant's arguments, see "Remarks" section of the response filed 9/24/2007, with respect to the rejection(s) of claim(s) 1-14 under 35 U.S.C. §102(b) have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of §102(e) under Beletsky et al. as discussed below.

All previously outstanding objections and rejections to the Applicant's disclosure and claims not contained in this Action have been respectfully withdrawn by the Examiner hereto.

Information Disclosure Statement

The IDS filed 9/24/2007 has be acknowledged by the Examiner. A signed copy has been included herewith.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 5, it is not clear how the data rearrangement information may contain an address of the second data storage section as well as also be able to address the data stored in the first data storage section (limitation 'd' of parent claim 4), as the limitations appear to conflict with each other. Essentially, it is not clear how an address of the second data storage section (claim 5) can also address data stored in the first data storage section (claim 4). Nonetheless, for the purposes of examination, the Examiner has considered claim 5 to read "wherein the data storage rearrangement information contains an address of the second first data storage section."

Claim 6 is rejected as being dependent upon rejected base claim 5.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-11 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Beletsky et al (U.S. Patent Application Publication No. 2004/0148153).

As per claims 1 and 8, Beletsky teaches **a method for rearranging data comprising the steps of:**

a) storing a plurality of data (shadow read data) **in a first data storage section** (first column portion of circular buffer 40 - figure 6) - ¶65 teaches reading data from the address via a read port of a RAM (¶13) and storing the read out data in circular buffer**;**

b) storing data rearrangement information (the address associated with each data entry of circular buffer 40 - figure 6) **in a stack** (as circular buffer 40, itself, may be considered a LIFO buffer, ¶65, it can therefore be seen that the data portion column is operated as a stack since stacks operate on the same "last-in, first-out" functionality)**;**

c) reading the data stored in the first data storage section (during a rewind period, ¶62, data is read out from the circular buffer first column portion) **, and storing the data in a rearranged order** (data is considered to be stored in the RAM in a "rearranged order" when taken in reference with the order of the data when stored in the circular buffer 40) **in a second data storage section** (system RAM via RAM's write port 20, figure 1) **based on the data rearrangement information stored in the stack** (address data from second column portion of the circular buffer 40 - figure 6 - is used to store the corresponding data to a specific address back in RAM - ¶63) In other words, during random writes to the RAM, data that is to be overwritten is stored in the circular buffer 40 in order to be rewound at a later point. This data is stored in a last-in, first-out order within circular buffer 40 as discussed. When data is rewound, and therefore stored back in the RAM, the data will be written back to its original location in the order the system originally over-wrote the data. Therefore, since the data is stored in the circular buffer in the order by which it is overwritten during writes to the RAM, and since data can be stored in any order in RAM, according to the program write instructions that are being executed

by the system, it can therefore be seen that the data stored in the circular buffer will be stored back in the RAM in a different order that it was stored in the circular buffer 40.

d) addressing the data stored in the second data storage section by the data rearrangement information (data may be addressed in the second storage section via the data in the rearrangement information as the rearrangement information, itself, is the corresponding address of each data element that is rewritten into RAM during the rewind periods - ¶62).

As per claims 2 and 9, Beletsky teaches **wherein the data rearrangement information contains an address of the second data storage section** (the address data of the second column of the circular buffer - figure 6 - comprises address data of the RAM {second data storage section} that corresponds to the data of the first column of the buffer 40 - ¶65.

As per claim 3, Beletsky teaches **wherein the first data storage section is a register** (it is well known in the art that DRAM, which the circular buffer comprises (¶57) is a collection of registers, which may be organized into rows. Thus the first data storage section may be considered a register when only one entry is written into the circular buffer before a rewind procedure is executed (e.g. the first entry of column one of the circular buffer shown in figure 6 comprises a register that stores data D1).

Beletsky also teaches the **second data storage section is a RAM** (a DRAM is a type of RAM as known in the art - ¶57).

As per claim 4, Beletsky teaches a **method for rearranging data comprising the steps of:**

a) storing a plurality of data in a first data storage section (data is written to system RAM - ¶13);

b) storing data rearrangement information in a stack (address data is stored into stack 40, as the circular buffer 40 may be a LIFO - ¶65);

c) reading the plurality of data stored in the first data storage section in an order based on the data rearrangement information stored in the stack (data is read from the RAM in an order based on the rearrangement information in the stack 40 since the rearrangement data is stored in the stack whenever a shadow read is made to the RAM - ¶65; therefore, the order data is read out from the RAM is *based* on the order the data rearrangement information in the stack is stored since when data is read from the RAM, it is immediately stored in a LIFO arrangement in the circular buffer 40, making the order data was read out the same as the order in which the data is stored in the buffer 40), **and storing the data in a rearranged order in a second data storage section** (similar to the discussion of claim 1 above, when data is written randomly to system RAM, a shadow read to the address captures the data to be overwritten and stores this data and the address in LIFO 40. Therefore, the data of LIFO is stored in an order based on program execution of stores that overwrite locations of the system RAM while the order of the data of the system RAM is stored based on linearly increasing address (0x000, 0x001, etc) as well known in the art of RAM addressing; thus when the data is written to the LIFO, it can be seen that it will be stored in a different order than the order of the data within the system RAM; **and**

d) addressing the data stored in the first data storage section by the data rearrangement information (since the data rearrangement information is the address of RAM for corresponding data, the data in the RAM {first data storage} is addressed by its respective address {rearrangement information} of the RAM).

As per claim 5, Beletsky teaches **the data rearrangement information contains an address of the first data storage section** (the data rearrangement information is address data of the RAM data entries and are stored in the circular buffer 40 as shown in figure 6).

As per claim 6, **the first data storage section is a RAM** (¶13) and the **second data storage section is a register** (as discussed with respect to claim 3 above) RAM may be organized in a collection of rows, or registers. Thus the second data storage section may be considered a register when only one entry is written into the circular buffer before a rewind procedure is executed (e.g. the first entry of column one of the circular buffer shown in figure 6 comprises a register that stores data D1).

As per claims 7 and 10, **the first and second data storage sections are RAMs** - (¶13 and ¶57).

As per claim 11, Beletsky teaches **wherein the reading and the storing are carried out by using an address conversion table** (the Examiner is considering the collection of data rearrangement entries corresponding to a single rewind interval (see figure 7) to be an address conversion table as it would comprise the collection of address of the system RAM that have had their corresponding data entries converted or overwritten with new data) **and a corresponding stack pointer** (the state machine 45 - figure 1 - controls a stack pointer as taught in ¶61, that is used during the reading of data from the stack 40 into the RAM).

As per claim 14, Beletsky teaches **data stored in the address conversion table** (collection of data rearrangement entries corresponding to a single rewind interval) **includes byte write information** (the addresses of the RAM that are stored as rearrangement data may be

considered "byte write information" as they indicate the addresses of system RAM whose bytes of data have been overwritten with new data).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beletsky et al. (U.S. Patent Application Publication No. 2004/0148153).

As per claim 12, Beletsky teaches in ¶61 using a state machine 45 to increment or decrement a stack pointer but does not specifically teach **using logic OR or logic ADD operation of a read address and an offset register**. Decrementing a pointer is well known in the art and it would have been obvious to one having ordinary skill in the art at the time of invention to have realized that in order to decrement an address of the stack pointer during a rewind operation, the state machine 45 would use an **ADD operation** to add a 2's compliment of an **offset** (e.g. the negative value of the address offset) to a previous **read address** to acquire the new address of the entry in the stack 40 to read. One of ordinary skill in the art would have recognized that the offset register could be any register that held the address offset between consecutive entries in the stack (usually 1).

Allowable Subject Matter

Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

As per claim 13, neither Beletsky or the prior art of record specifically teach or suggest, either alone or in combination, the limitation of the reading and storing steps being carried out using a register instead of a stack pointer. Beletsky teaches using a stack pointer generated by state machine 45 in ¶61 but does not mention the use of substituting the stack pointer for a register.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Shane M. Thomas
Patent Examiner

5 November 2007